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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Moshe Stark

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24505

7590

10/05/2006

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EXAMINER

DANIELS, ANTHONY J

ART UNIT

PAPER NUMBER

2622

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/993,917	<b>Applicant(s)</b> STARK, MOSHE	
	<b>Examiner</b> Anthony J. Daniels	<b>Art Unit</b> 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 11 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/11/2006 has been entered.

### ***Response to Arguments***

2. Applicant's arguments filed 9/11/2006 regarding whether the Sauer et al. reference is summing or averaging charges have been fully considered but they are not persuasive. The examiner has stated his position on this matter numerous times throughout prosecution. Sauer et al. clearly states summing the charges. Nowhere in the Sauer et al. reference is averaging suggested.

3. Applicant's arguments filed 9/11/2006 regarding the whether or not the unit cells of Sauer et al. are unit cells have been fully considered and are persuasive. A new grounds of rejection is being made for the independent claims.

### ***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

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4. Claims 1,12,23,24,26,27,34,35,37,38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. (US # 5,973,311). *Note the interchangeability of lines and columns in claims 24,26,35,37.*

As to claim 1, Sauer et al. teaches an active pixel image sensor (Figure 2, Figure 4, pixel elements “22” containing transistors “TR11” and “TC11”; *{The active elements, i.e. transistors “TC11”, “TR11”, define the sensor as an active pixel image sensor.}*) comprising: a plurality of unit cells (Figure 4, pixel elements “22”; reset “66”, “68”), each adapted to generate charge in response to photons incident thereon (Col. 4, Lines 14-21; Col. 7, Lines 27-32); and array elements adapted to sum charge from one or more unit cells at the focal plane of said image sensor (Col. 4, Lines 22-30; Lines 38-44; Col. 7, Lines 27-32). Although Sauer et al. does not state it explicitly, **Official Notice** is taken that direct injection unit cells are well known and expected in the art. One of ordinary skill in the art would have motivated to implement direct injection unit cells as the unit cells in Sauer et al., because direct injection unit cells mitigate blooming effects in CMOS sensors.

As to claim 12, Sauer et al. teaches an active pixel image sensor (Figure 2, Figure 4, pixel elements “22” containing transistors “TR11” and “TC11”; *{The active elements, i.e. transistors “TC11”, “TR11”, define the sensor as an active pixel image sensor.}*) comprising: a plurality of direct injection unit cells (Figure 1, pixel elements “22”; reset “66”, “68”), each adapted to generate charge in response to photons incident thereon (Col. 4, Lines 14-21); and array elements adapted to change resolution of the output image of said image sensor at a focal plane of said image sensor (Col. 4, Lines 14-17; Lines 62-64) by summing the charge generated by one or more unit cells of said plurality of unit cells (Col. 4, Lines 64-67; Col. 7, Lines 14-32). Although

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Sauer et al. does not state it explicitly, **Official Notice** is taken that direct injection unit cells are well known and expected in the art. One of ordinary skill in the art would have motivated to implement direct injection unit cells as the unit cells in Sauer et al., because direct injection unit cells mitigate blooming effects in CMOS sensors.

As to claim **23**, claim 23 is a method claim corresponding to apparatus claim 1. Therefore, method claim 23 is analyzed and rejected as previously discussed with respect to the apparatus claim 1.

As to claim **24**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises: activating charge transfer transistors of one or more lines of unit cells (Figure 2, "Column Select Line 1" and transistor "TC11"); Col. 5, Lines 23-29; *{Activating column select line 1, in turn, activates the aforementioned transistor of Figure 2.}*); activating one or more columns of unit cells (Figure 4, "Row Select Line 1" and "Row Select Line 2"; Col. 7, Lines 27-32); and combining the charge transferred by activated charge transfer transistors of said activated columns (Col. 7, Lines 24-32).

As to claim **26**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises activating one line and combining charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (Col. 4, Lines 45-67).

As to claim **27**, Sauer et al. teaches a method according to claim 23 and wherein said summing comprises activating U adjacent lines and combining charge of V columns thereby to combine charge from UxV unit cells in a UxV block (Col. 7, Lines 14-32).

As to claim 34, claim 34 is a method claim corresponding to apparatus claim 12. Therefore, method claim 34 is analyzed and rejected as previously discussed with respect to the apparatus claim 12.

As to claim 35, the limitations in claim 35 can be found in claim 24. Therefore, claim 35 is analyzed and rejected as previously discussed with respect to claim 24.

As to claim 37, the limitations in claim 37 can be found in claim 26. Therefore, claim 37 is analyzed and rejected as previously discussed with respect to claim 26.

As to claim 38, the limitations in claim 38 can be found in claim 27. Therefore, claim 38 is analyzed and rejected as previously discussed with respect to claim 27.

5. Claims 2,4,5,13,15,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. (see Patent Number above) in view of Kokie et al. (US #4,212,034). *Note the interchangeability of rows and columns in claims 2,4,13,15.*

As to claim 2, Sauer et al. teaches an image sensor according to claim 1 (see above 102(b) rejection) and wherein said array elements comprise: charge transfer transistors (see Figure 2, Reference Number "TC11") adapted to transfer charge when activated (see Col. 5, Lines 23-29); a line decoder (see Figure 4, Reference Number "50"; *{Horizontal Shift Register (50) performs same task as line decoder; see Col. 6, Lines 62-65.}*) adapted to activate charge transfer transistors of one or more lines of unit cells (see Col. 6, Lines 62-65; *{Activating column select line 1, in turn, activates the aforementioned transistor of Figure 2.}*); and a column selector (see Figure 4, Reference Number "48"; *Vertical Shift Register (48) performs same task as column selector; see Col. 6, Lines 60-62.}*) adapted to activate one or more columns of unit

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cells and to combine the charge transferred by activated charge transfer transistors of said activated columns (see Col. 4, Lines 62-67; Col. 6, Lines 11-20). The claim differs from Sauer et al. in that it requires one charge transfer transistor per unit cell.

In the same field of endeavor, Kokie et al. teaches unit cells (see Figure 1, Reference Numbers "4-1 – 4-4") containing one charge transfer transistor (see Figure 1, Reference Number "5") per unit cell transferring charge from photo detectors (PD4-1 – PD4-4). In light of the teaching of Kokie et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to include only one charge transfer transistor per unit cell. One transistor per unit cell would decrease space taken up by the unit cell and; subsequently, the array, and one transistor per unit cell would allow for more efficient operation of the array; meaning, not having to activate two transistors to transfer charge from one unit cell as taught by Sauer et al.

As to claim 4, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2 (see above 103(a) rejection) and wherein said array elements comprise adjacent column means (see Sauer et al., Figure 2, Clock Input Signals "52" and "54"; Col. 6, Lines 62-65) adapted to indicate to said line decoder to activate one line and to said column selector to combine charge of at least two columns thereby to combine charge from at least two unit cells in adjacent columns (see Sauer et al., Col. 4, Lines 45-67).

As to claim 5, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2 (see 103(a) rejection above) and wherein said array elements comprise block means adapted (see Sauer et al., Figure 4, Clock Input Signals "52" and "54") to indicate to said line decoder to activate U adjacent lines and to said column selector to combine charge of V columns thereby to combine charge from UxV unit cells in a UxV block (see Col. 7, Lines 14-32).

As to claim 13, the limitations in claim 13 can be found in claim 2. Therefore, claim 13 is analyzed and rejected as previously discussed with respect to claim 2.

As to claim 15, the limitations in claim 15 can be found in claim 4. Therefore, claim 15 is analyzed and rejected as previously discussed with respect to claim 4.

As to claim 16, the limitations in claim 16 can be found in claim 5. Therefore, claim 16 is analyzed and rejected as previously discussed with respect to claim 5.

6. Claims 3,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Kokie et al. (see Patent Numbers above), and further in view of Pain et al. (US #8,801,258).  
*Note the interchangeability of rows and columns in claims 3 and 14.*

As to claim 3, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 2, and wherein said array means comprise adjacent line means adapted to provide indications to the line decoder and the column selector (see 103(a) rejection above), but the claim differs from Sauer et al., as modified by Kokie et al., in that it requires that the provided indications to said line decoder activate at least two adjacent lines and to said column selector select one column thereby to combine charge from the corresponding unit cells in adjacent lines.

In the same field of endeavor, Pain et al. teaches the activation of a column and at least two adjacent lines, noting interchangeability, whereupon the charges are combined from the corresponding unit cells in the at least two adjacent lines (see Col. 2, Lines 59-67, Col. 3, Lines 1-9). In light of the teaching of Pain et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to activate a column and at least two adjacent lines, whereupon charges are combined from the corresponding unit cells in the at least two adjacent



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lines. Such activations would allow for two methods of combining charges to be used, 1) activation of two columns and one line and summing as described in claim 4, 2) activation of one column and two lines and summing described by Pain et al.; thus, receiving different signal-to-noise ratios for each method, comparing them, and using the highest to have the sensor operate with an optimal signal-to-noise ratio with little or no change in resolution.

As to claim 14, the limitations in claim 14 can be found in claim 3. Therefore, claim 14 is analyzed and rejected as previously discussed with respect to claim 3.

7. Claims 6,7,17,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al., Kokie et al., and Pain et al. (see Patent Numbers above), and further in view of Nishida et al. (US #4,996,600). *Note interchangeability of rows and columns in claims 6,7,17,18. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim 6, Sauer et al., as modified by Kokie et al. and Pain et al., teaches an image sensor according to claim 3 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al. and Pain et al., in that it requires interlace means adapted to produce video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches an interlace means (see Figure 15, Reference Numbers “103, “114”) adapted to produce video output from said image sensor (see Col. 3, Lines 26-34) in an interlace mode (see Figure 1). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include interlace means adapted to produce video output from said image sensor in an interlace mode. Such a means would allow for a sufficiently large charge with little noise to be

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obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim 7, Sauer et al., as modified by Kokie et al., Pain et al., and Nishida et al., teaches that said interlace means comprise means adapted to activate said adjacent line means to combine charge of pairs of unit cells in adjacent lines beginning with odd lines (see Nishida et al., Figure 1, Reference Numbers "P1-1", "P2-1" and "P3-1", "P4-1"; sampling points in first field) adapted to an odd field output and of adjacent lines beginning with the even lines (see Nishida et al., Figure 1, Reference Numbers "P2-2", "P3-2" and "P4-2", "P5-2"; sampling points in second field) adapted to an even field output.

As to claim 17, the limitations in claim 17 can be found in claim 6. Therefore, claim 17 has been analyzed and rejected as previously discussed with respect to claim 6.

As to claim 18, the limitations in claim 18 can be found in claim 7. Therefore, claim 18 has been analyzed and rejected as previously discussed with respect to claim 7.

8. Claims 8-11, 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Kokie et al. (see Patent Numbers above), and further in view of Nishida et al (see Patent Number above). *Note the interchangeability of rows and columns in claims 8, 9, 19, 20. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim 8, Sauer et al., as modified by Kokie et al., teaches an image sensor of claim 4 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al., in that it requires intercolumn means adapted to produce video output from said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches an intercolumn means (see Figure 15, Reference Number “103”, “114”) adapted to produce video output from said image sensor (see Col. 3, Lines 26-34) in an intercolumn mode (see Figure 6A and 6B). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to include intercolumn means adapted to produce video output from said image sensor in an intercolumn mode. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim 9, Sauer et al., as modified by Kokie et al. and Nishida et al., teaches that said intercolumn means comprises means adapted to activate said adjacent column means to combine charge of pairs of adjacent columns beginning with odd columns (see Figure 6B) adapted to an odd field output and of adjacent columns beginning with even columns (see Figure 6A) adapted an even field output.

As to claim 10, Sauer et al., as modified by Kokie et al., teaches an image sensor according to claim 3 (see 103(a) rejection above). The claim differs from Sauer et al., as modified by Kokie et al., in that it requires block interlace means adapted to produce video output from said image sensor in an block interlace mode.

In the same field of endeavor, Nishida et al. teaches an block interlace means (see Figure 15, Reference Number “103”, “114”) adapted to produce video output from said image sensor (Col. 3, Lines 26-34) in an block interlace mode (see Figure 1). In light of the teaching of Nishida et al. it would have been obvious to one of ordinary skill in the art at the time the

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invention was made to include block interlace means adapted to produce video output from said image sensor in an block interlace mode. Such a means would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim 11, Sauer et al., as modified by Kokie et al and Nishida et al., teaches that said block interlace means comprise means adapted to activate said block means to combine charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper-left hand unit cell is in the first column, first line (see Figure 1, sampling points in the first field) and wherein the blocks of an even field output begin with the block whose upper-left hand unit cell is in the second column, second line (see Figure 1, sampling points of second field).

As to claim 19, the limitations in claim 19 can be found in claim 8. Therefore, claim 19 has been analyzed and rejected as previously discussed with respect to claim 8.

As to claim 20, the limitations in claim 20 can be found in claim 9. Therefore, claim 20 has been analyzed and rejected as previously discussed with respect to claim 9.

As to claim 21, the limitations in claim 21 can be found in claim 10. Therefore, claim 21 has been analyzed and rejected as previously discussed with respect to claim 10.

As to claim 22, the limitations in claim 22 can be found in claim 11. Therefore, claim 22 has been analyzed and rejected as previously discussed with respect to claim 11.

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9. Claims 25,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. (see Patent Number above) in view of Pain et al. (see patent Number above). *Note the interchangeability of rows and columns in claims 25,36.*

As to claim 25, Sauer et al. teaches a method according to claim 23 (see 102(b) rejection above), wherein summing comprises activation of certain lines and columns thereby to combine charge from the corresponding lines or columns, but the claim differs from Sauer et al. in that it requires, specifically, the activation of least two lines and the selection of one column thereby to combine charge from the corresponding unit cells in adjacent lines.

In the same field of endeavor, Pain et al. teaches the activation at least two adjacent lines and the selection of one column thereby to combine charge from the corresponding unit cells in adjacent lines (see Col. 2, Lines 59-67, Col. 3, Lines 1-9). In light of the teaching of Pain et al. it would have been obvious to one of ordinary skill in the art at the time the invention was made to activate a column and at least two adjacent lines, whereupon charges are combined from the corresponding unit cells in the at least two adjacent lines. Such activations would allow for two methods of combining charges to be used, 1) activation of two columns and one line and summing, 2) activation of one column and two lines and summing; thus, receiving different signal-to-noise ratios for each method, comparing them, and using the highest to have a device with a more optimal signal-to-noise ratio with little or no change in resolution.

As to claim 36, the limitations in claim 36 can be found in claim 25. Therefore, claim 36 has been analyzed and rejected as previously discussed with respect to claim 25.

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10. Claims 28,29,39,40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. and Pain et al. (see Patent Numbers above), and further in view of Nishida et al. (see Patent Number above). *Note the interchangeability rows and columns in claims 28,29,39,40. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim **28**, Sauer et al., as modified by Pain et al., teaches a method according to claim 25 (see 103(a) rejection above), but the claim differs from Sauer et al., as modified by Pain et al., in that the method comprises producing video output from said image sensor in an interlace mode.

In the same field of endeavor, Nishida et al. teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in an interlace mode (see Figure 1). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an interlace mode. . Such a modification would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **29**, Sauer et al., as modified by Pain et al. and Nishida et al., teaches a method according to claim 28 (see 103(a) rejection above) and wherein said producing comprises combining charge of pairs of unit cells in adjacent lines beginning with odd lines (see Nishida et al., Figure 1, Reference Numbers “P1-1”, “P2-1” and “P3-1”, “P4-1”; sampling points in first field) for an odd field output and of adjacent lines beginning with even lines (see Nishida et al., Figure 1, Reference Numbers “P2-2”, “P3-2” and “P4-2”, “P5-2”; sampling points in second field) for an even field output.

As to claim 39, the limitations in claim 39 can be found in claim 28. Therefore, claim 39 has been analyzed and rejected as previously discussed with respect to claim 28.

As to claim 40, the limitations in claim 40 can be found in claim 29. Therefore, claim 40 has been analyzed and rejected as previously discussed with respect to claim 29.

11. Claims 30-33, 41-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sauer et al. in view of Nishida et al. (see Patent Numbers above). *Note the interchangeability of rows and columns in claims 30-33, 41-44. Also note Col. 7, Lines 34-38 in Nishida et al. when considering 4,996,600 as prior art.*

As to claim 30, Sauer et al. teaches a method according to claim 26 (see 102(b) rejection), but the claim differs from Sauer et al. in that the method comprises producing video output from said image sensor in an intercolumn mode.

In the same field of endeavor, Nishida et al. teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in an intercolumn mode (see Figure 6A and 6B). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an intercolumn mode. Such a modification would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim 31, Sauer et al., as modified by Nishida et al., teaches a method according to claim 30 (see 103(a) rejection above) and wherein said producing comprises combining charge

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of pairs of adjacent columns beginning with odd columns (see Figure 6B) for an odd field output and of adjacent columns beginning with even columns (see Figure 6A) for an even field output.

As to claim **32**, Sauer et al., as modified by Nishida et al., teaches a method according to claim 31 (see 103(a) rejection above), but the claim differs from Sauer et al., as modified by Nishida et al., in that the method requires producing video output from said image sensor in a block interlace mode.

In the same field of endeavor, Nishida et al., also teaches producing video output from said image sensor (see Col. 3, Lines 26-34) in a block interlace mode (see Figure 1). In light of the teaching of Nishida et al., it would have been obvious to one of ordinary skill in the art at the time the invention was made to produce video output from said image sensor in an block interlace mode. Such a modification would allow for a sufficiently large charge with little noise to be obtained, increased dynamic range and; consequently, high-quality reproduced images, with reduced residual images, can be obtained (see Nishida et al., Col. 2, Lines 43-48).

As to claim **33**, Sauer et al., as modified by Nishida et al., teaches a method according to claim 32 (see 103(a) rejection above) and wherein said producing comprises combining charge of 2x2 blocks wherein the blocks of an odd field output begin with the block whose upper-left hand unit cell is in the first column, first line (see Figure 1, sampling points in the first field) and wherein the blocks of an even field output begin with the block whose upper-left hand unit cell is in the second column, second line (see Figure 1, sampling points of second field).

As to claim **41**, the limitations in claim 41 can be found in claim 30. Therefore, claim 19 has been analyzed and rejected as previously discussed with respect to claim 30.



As to claim 42, the limitations in claim 42 can be found in claim 31. Therefore, claim 42 has been analyzed and rejected as previously discussed with respect to claim 31.

As to claim 43, the limitations in claim 43 can be found in claim 32. Therefore, claim 43 has been analyzed and rejected as previously discussed with respect to claim 32.

As to claim 44, the limitations in claim 44 can be found in claim 33. Therefore, claim 44 has been analyzed and rejected as previously discussed with respect to claim 33.


### *Conclusion*

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Daniels whose telephone number is (571) 272-7362. The examiner can normally be reached on 8:00 A.M. - 5:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AD  
09/22/06

  
NGOC-YEN VU  
SUPERVISORY PATENT EXAMINER